MANUAL

JK-310

JK AUDIO

CAUTION!

STATIC ELECTRICITY CAN DESTROY SOME INTEGRATED CIRCUITS ON THE JK-310 AND ALSO YOUR COMPUTER.

NEVER CONNECT OR DISCONNECT YOUR JK-310 TO YOUR COMPUTER WHEN THE POWER IS APPLIED TO EITHER ONE OF THEM.

THE POWER SUPPLY CAN BE CONNECTED TO THE USER PORT CONNECTOR (44 PIN STANDARD) OR STRAIGHT TO THE COMPUTER AS NORMAL. IF THE POWER CUBE THAT IS CONNECTED DIRECTLY TO THE COMPUTER IS USED THEN THE RESET SWITCH WILL NOT WORK CORRECTLY. THE RESET SWITCH IN THE JK-310 IS USED TO KEEP POWER TO THE INTERFACE BOARD ON (THIS KEEPS THE SAME STATE OF THE OUTPUT LATCHES) AND RESET OR TURN OFF THE COMPUTER. UP IS ON AND DOWN IS OFF.

HOW DOES IT WORK

LET'S IMAGINE THAT YOU WANT LIGHTS OR INDICATORS ON ALL THE OUTPUT LINES AND YOU WANT TO LABEL THEM 1 THOUGH 8. SUPPOSE YOU WANTED LIGHT #6 ON AND ALL THE REST OFF.

```
10 POKE 16382,1
```

THIS SETS UP A CONTROL WORD ON THE I/O BOARD AND LETS IT KNOW THAT YOU WANT TO TALK TO THE OUTPUT PORT.

```
20 POKE 16383,32
```

THIS SENDS OUT BINARY NUMBER 32 (LIGHT #6 ON) WHICH HAS BEEN DIRECTED TO THE OUTPUT PORT IN LINE 10.

THAT'S IT!

IF YOU WANT MORE THAN ONE LIGHT ON AT A TIME THEN SIMPLY ADD UP THE X'S.

INPUT PORT

THE INPUT PORTS WORK IN A VERY SIMILAR MANNER. SUPPOSE YOU HAD 8 SWITCHES, S1-S8, AND YOU WANTED TO CHECK THE STATE OF ALL OF THEM AND SEE IF THEY HAVE BEEN ACTIVATED.

SOFTWARE

```
PRINT PEEK 16382
```

IF AN 8 IS PRINTED ON THE SCREEN THEN WE KNOW THAT SWITCH #4 IS ACTIVATED BY LOOKING IN THE BINARY TABLE. IF A 162 (128+32+2) WAS PRINTED THEN WE KNOW THAT SWITCHES #8, #6, AND #2 ARE ACTIVATED.

BINARY TABLE

PORT		PORT	
0 1	x=1	6 7	x=64
1 2	x=2	7 8	x=128
2 3	x=4	1 and 4	x= 9
3 4	x=8	7 and 4	x=72
4 5	x=16	3 and 8	x=132
5 6	x=32	5 and 6	x=48

HARDWARE

THE EDGE CONNECTOR THAT ALL THE I/O PORT AND CONTROL SIGNALS ARE CONNECTED TO IS

THE STANDARD 44 PIN .156 SPACING WHICH RADIO SHACK SELLS CAT. #(276-1551). THE REASON THIS CONNECTOR IS USED IS BECAUSE RADIO SHACK SELLS EXPERIMENTER CARDS THAT YOU CAN USE TO BUILD UP YOUR OWN IDEAS.

WITH NOTHING ON INPUTS, PEEK 16382 = 255
⇒ ANY INPUT FLOATING IS READ AS HIGH LEVEL

CLOCK/CALENDAR

THE CLOCK/CALENDAR IS ADDRESSED AT 16380 AND 16381. POKING NUMBERS OUT AT 16380 (CLOCK CONTROL) WILL ALLOW YOU TO READ OR WRITE CERTAIN FUNCTIONS.

```
EXAMPLE   SET CLOCK
POKE 16380, (F+64)          <F= FUNCTION NUMBER>
POKE 16381, D               <D= CLOCK/CALENDAR DATA>
POKE 16380,(F+80)
POKE 16380, 0
```

THESE STEPS SET UP ONLY ONE FUNCTION AND HAVE TO BE REPEATED TO SET THE ENTIRE CLOCK/CALENDAR. IN THE NEXT EXAMPLE WE WILL SET THE ONES PLACE OF THE MINUTES TO A 7.

```
EXAMPLE                     (XX:X7:XX)

POKE 16380, (2+64)      (THE 2 IS THE FUNCTION #
                        OF THE ONES PLACE IN THE MIN. <M1>)
POKE 16381, 7           DATA
POKE 16380, (2+80)
POKE 16380, 0
```

READ CLOCK/CALENDAR

READING THE CLOCK IS SIMILAR TO SETTING IT AND IS DONE A FUNCTION AT A TIME.

```
GENERAL EXAMPLE
POKE 16380, 96
POKE 16380, 96+F        F= THE FUNCTION
LET D = PEEK 16381      D= DATA
POKE 16380, 0
```

```
EXAMPLE
READ THE TENS PLACE IN MINUTES.      (XX:DX:XX)
POKE 16380, 96
POKE 16380, 96+3
LET D= PEEK 16381
POKE 16380, 0
```

IN THIS CASE IF THE CLOCK READS 27 MINUTES 'D' WOULD EQUAL 2

HERE ARE SOME SUBROUTINES TO SET AND READ THE CLOCK. S1 AND S10 ARE RESET TO 0 IRRESPECTIVE OF INPUT DATA WHEN ADDRESSING FUNCTIONS 0 AND 1. THERE ARE TWO WAYS TO READ THE CLOCK SUBROUTINE PROGRAM. THE FIRST WAY IS TO READ IT DIRECTLY FROM THE ARRAY. THE SUBSCRIPT IN THE ARRAY (NUMBER IN PARENTHESIS) IS ONE GREATER THAN THE FUNCTION. FOR EXAMPLE, IF YOU WANT TO READ THE ONES PLACE IN THE HOURS THIS WOULD BE FUNCTION #4, BUT THE SUBSCRIPT NUMBER THAT GOES IN THE ARRAY WOULD BE 5. T$(5)=H1 THIS WAY USES LESS MEMORY BECAUSE YOU CAN ELIMINATE LINES 8300 - 8330 AND 7100 - 7130 AND CHANGE LINE 8095 TO '8095 RETURN '. THE SECOND WAY TO READ THE CLOCK/CALENDAR IS TO USE THE VARIABLES WHICH COMBINES THE ONES AND TENS PLACE OF EACH JUNCTION.

```
ASSIGNED VARIABLES
SE = SECONDS            WE = WEEK (0-6)
MI = MINUTES            DA = DAY
HO = HOURS              MO = MONTH
M$ = MODE (AM,PM,24)    YE = YEAR
                        L$ = LEAP YEAR
```

8K ROM; 2K RAM

THE CLOCK AND CALENDAR SUBROUTINES ARE SEPARATED TO SAVE MEMORY IF ONE IS NOT NEEDED. THESE SUBROUTINES ALONG WITH THE MAIN PROGRAM WILL PRINT OUT THE TIME AND DATE AT THE TOP OF THE SCREEN.

MAIN

```
100 GOSUB 8000
103 CLS
104 PRINT " "
105 PRINT T$(6);T$(5);":";T$(4)
;T$(3);":";T$(2);T$(1);" ";M$
200 GOSUB 7000
215 PRINT
220 PRINT WE;" ";MO;"/";DA;"/";
YE
225 IF INKEY$="A" THEN STOP
230 GOTO 100
```

DATE

```
7000 DIM T$(13)
7010 FOR F=6 TO 12
7020 POKE 16380,96
7030 POKE 16380,96+F
7040 LET ZQ=PEEK 16381
7050 POKE 16380,0
7060 LET NQ=F+1
7070 IF F=8 THEN GOSUB 7900
7080 LET T$(NQ)=STR$ ZQ
7090 NEXT F
7100 LET WE=VAL T$(7)
7110 LET DA=10*(VAL T$(9))+VAL T
$(8)
7120 LET MO=10*(VAL T$(11))+VAL
T$(10)
7130 LET YE=10*(VAL T$(13))+VAL
T$(12)
7900 IF ZQ>=4 THEN GOTO 7930
7910 LET L$="NOT LEAP YEAR"
7920 RETURN
7930 LET L$="LEAP YEAR"
7940 LET ZQ=ZQ-4
7950 RETURN
```

TIME

```
8000 DIM T$(6)
8010 FOR F=0 TO 5
8020 POKE 16380,96
8030 POKE 16380,96+F
8040 LET ZQ=PEEK 16381
8050 POKE 16380,0
8060 LET NQ=F+1
8070 IF F=5 THEN GOSUB 8100
8080 LET T$(NQ)=STR$ ZQ
8090 NEXT F
8095 GOTO 8300
8100 IF ZQ>=8 THEN GOTO 8120
8110 GOTO 8140
8120 LET M$="24"
8130 LET ZQ=ZQ-8
8140 LET M$="AM"
8150 IF ZQ>=4 THEN GOTO 8170
8160 RETURN
8170 LET M$="PM"
8180 LET ZQ=ZQ-4
8190 RETURN
8300 LET SE=10*(VAL T$(2))+VAL T
$(1)
8310 LET MI=10*(VAL T$(4))+VAL T
$(3)
8320 LET HO=10*(VAL T$(6))+VAL T
$(5)
8330 RETURN
```

±30 SEC.

```
9000 POKE 16380,128
9010 PRINT "30 SEC. RESET"
9020 POKE 16380,0
9030 STOP
```

8K ROM; 1K RAM

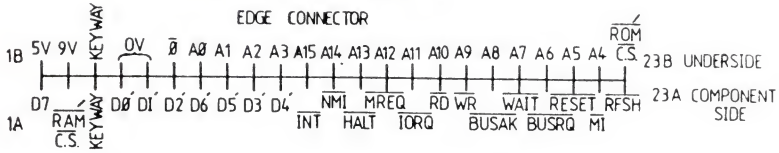
THE SET PROGRAM WORKS IN A SIMILAR MANNER AS THE READ PROGRAM (M1 IS F=3, M10 IS F=4, H1 IS F=5 ETC.). THE BATTERY BACK-UP WILL KEEP THE CLOCK GOING SO THIS PROGRAM SHOULDN'T BE USED TOO OFTEN.

EXAMPLE RUN PROGRAM AND SET TIME TO 06:27:00 AM

```
FUNCTION?
3
VALUE?
2 -
FUNCTION?
4
VALUE?
2 -
FUNCTION?
5
VALUE?
6 -
FUNCTION?
6
VALUE?
0 -
ENTER AM,PM, OR 24
"AM"
FUNCTION?
0     (TO END)
```

```
100 PRINT "FUNCTION?"
110 INPUT N
120 PRINT N
130 PRINT "VALUE"
140 INPUT V
150 PRINT V
160 LET F=N-1
170 IF F=-1 THEN STOP
180 IF F=5 THEN GOSUB 250
190 IF F=8 THEN GOSUB 300
200 POKE 16380,(F+64)
210 POKE 16381,V
220 POKE 16380,(F+80)
230 POKE 16380,0
240 GOTO 100
250 PRINT "ENTER AM,PM OR 24"
260 INPUT M$
270 IF M$="24" THEN LET V=V+8
280 IF M$="PM" THEN LET V=V+4
290 RETURN
300 PRINT "LEAP YEAR? (Y/N)"
310 INPUT L$
320 IF L$="Y" THEN LET V=V+4
330 RETURN
```

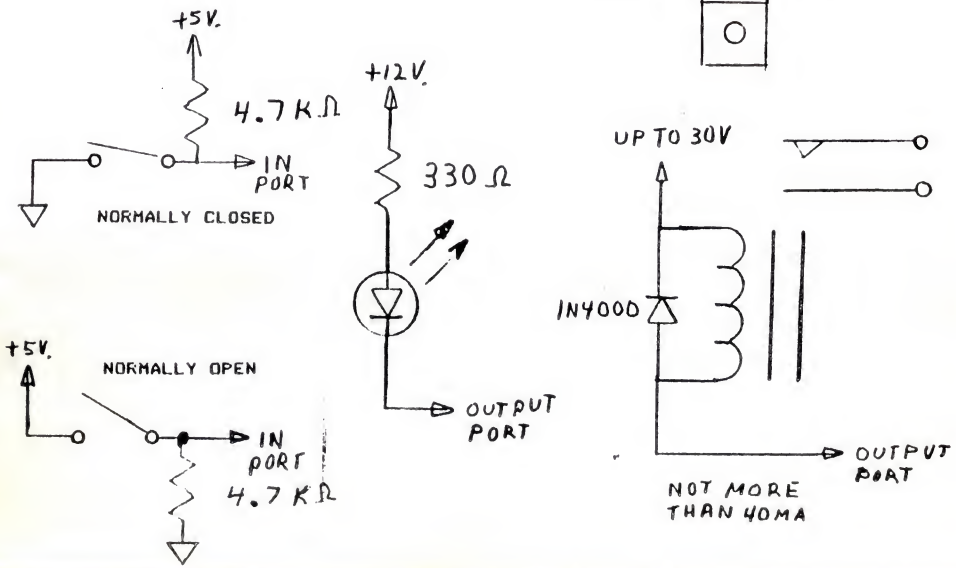
ZX-81 / TIMEX

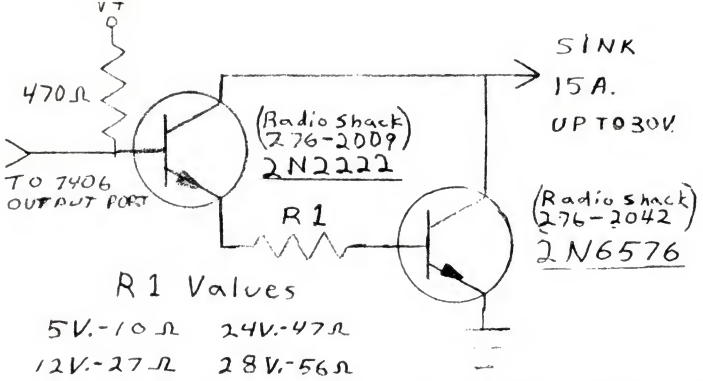


COMPONENTS SIDE TOP		BOTTOM
5 VOLTS	22	Z $\overline{2Y3}$
8 VOLTS	21	Y 1Y0
GND	20	X $\overline{1Y0}$
BATT. BACK UP	19	W 1Y3
30 SEC. CORRECTION	18	V $\overline{1Y3}$
OUTPUT (1)	17	U $\overline{2Y2}$
OUTPUT (0)	16	T D7'
OUTPUT (6)	15	S D6'
OUTPUT (7)	14	R D5'
OUTPUT (2)	13	P D4'
OUTPUT (5)	12	N D3'
OUTPUT (3)	11	M D2'
OUTPUT (4)	10	L D1'
INPUT (0)	9	K D0'
INPUT (1)	8	J D4
INPUT (2)	7	H D3
INPUT (3)	6	F D5
INPUT (4)	5	E D6
INPUT (5)	4	D D2
IUPUT (6)	3	C D1
IUPUT (7)	2	B D0
GND	1	A D7

PORT CONNECTOR

THE TOP OF THE EDGE CONNECTOR HAS ALL THE I/O PORTS AND POWER. THIS DESIGN WAS IMPLEMENTED SO THAT A SINGLE SIDED EDGE CONNECTOR COULD BE USED IF YOU WERE ONLY INTERESTED IN THE I/O PORTS. THE BOTTOM EDGE HAS NON-BUFFERED DATA LINES FOR INPUT DEVICES AND BUFFERED LINES FOR OUTPUT DEVICES. IT ALSO HAS ADDRESS SIGNALS SO THAT THE ACCESSORY BOARDS CAN RECEIVE THE CONTROL WORD.

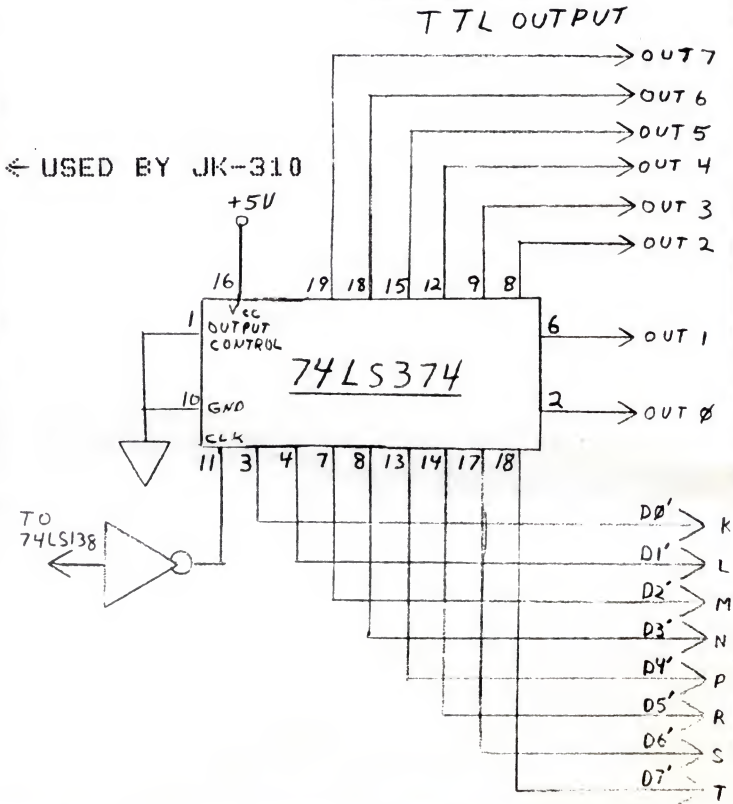


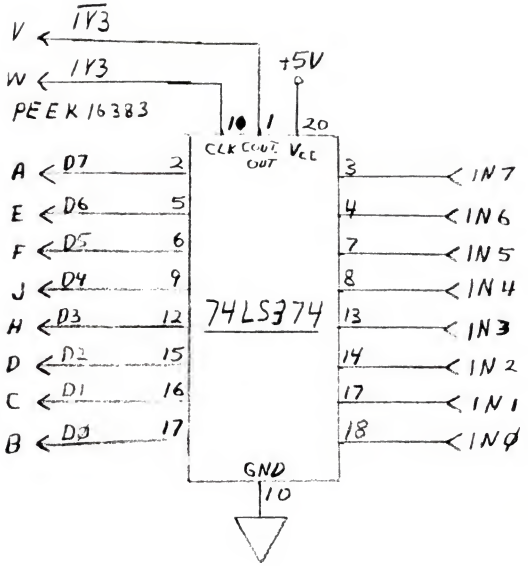


THE JK-310 IS EXPANDABLE WITH THE USE OF A CONTROL WORD. WE USE THE MIDDLE DIGIT OF THE MODEL NUMBER FOR THIS PURPOSE. THE REST OF THE NUMBERS ARE, SO FAR, ARE FREE TO USE FOR YOUR OWN ACCESSORIES. HERE ARE SOME SCHEMATICS OF EXTRA INPUT/OUTPUT PORTS. THE CONTROL WORD CAN BE CHANGED ON THE NEW PORT BY MOVING THE CONTROL LINE FROM THE (U13) 74LS374 TO DIFFERENT PINS ON THE (U11) 74LS138 (SEE TABLE).

WORD	PIN
Y0	15
Y1	14
Y2	13
Y3	12
Y4	11
Y5	10
Y6	9
Y7	7

← USED BY JK-310





MODIFICATION ZX-80 / MICROACE

THESE EARLY COMPUTERS DON'T HAVE A ROM C.S. ON THE EDGE CONNECTOR. LOCATE THE ROM IC ON THE PRINTED CIRCUIT BOARD. CUT THE FOIL THAT GOES TO PIN 20 (ROM C.S.) AND INSERT A 1K OHM RESISTOR. CONNECT A WIRE, ON THE ROM SIDE OF THE RESISTOR AND RUN IT TO PIN 23B ON THE EDGE CONNECTOR.

SPECIFICATIONS
MAIN BOARD JK-310

POWER USAGE @ 9 VOLTS	220 MA
RATING VOLTAGE	7-14 V
OPERATING TEMP	-30C TO +70C
CLOCK FREQUENCY	32.768 KHZ
CRYSTAL AGING FIRST 30 DAYS	3 PPM
FIRST YEAR	5 PPM
DECODING	MEMORY MAPPED
ADDRESSING	16380-16383
PC BOARD METERIAL	GLASS EPOXY
PC BOARD SIZE	7 7/8 IN. X 6 IN.
BATTERTY BACK UP	3 AA NICADS
BATTERY BACK UP TIME	TYP. 6 MO.
USER PORT CONNECTION	STANDARD 44 PIN .156 SPACING

7805
47µ
4K7
4K7
4K7
74LS175 U10
74LS374 U8
74LS06 U12
22µ
.01
.08
U11
74LS138
U9
74LS06
10K
37K
2N2222
100
10K
.01
U4
74LS139
U3
74LS04
TP1
2N2907
4µ7
Jumper
U5
74LS374
U2
74LS32
U1
74LS133
330

COMPONENT PLACEMENT	
JK 310	
.	9-16-82 SLC

OKI

semiconductor

MARCH 1980

MSM5832 MICROPROCESSOR REAL-TIME CLOCK/CALENDAR

GENERAL DESCRIPTION

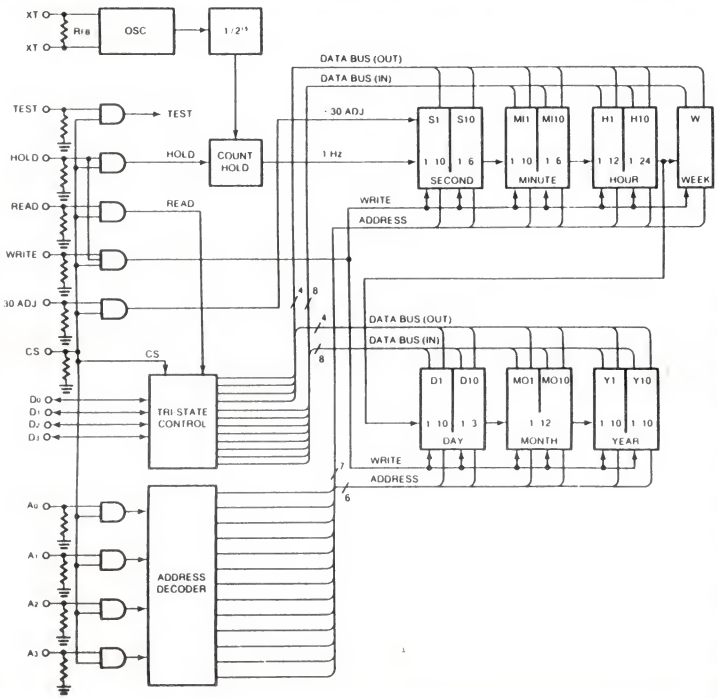
The MSM5832 is a monolithic, metal-gate CMOS integrated circuit that functions as a real time clock/calendar for use in bus-oriented microprocessor applications. The on-chip 32,768 Hz crystal controlled oscillator time base is counted down to provide addressable 4-bit I/O data of SECONDS, MINUTES, HOURS, DAY-OF-WEEK, DATE, MONTH, and YEAR. Data access is controlled by 4-bit address, chip select, read, write and hold inputs. Other functions include 12H/24H format selection, leap year identification and manual ± 30 second correction.

The MSM5832 normally operates from a 5 volt ± 5% supply. Battery back-up operation down to 2.2 volts allows continuation of time keeping when main power is off. One test input facilitates rapid testing of the time keeping operations. The MSM5832 is offered in an 18-lead dual-in-line plastic (RS suffix) package.

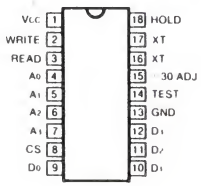
FEATURES

- Microprocessor bus-oriented
- TIME MONTH DATE YEAR DAY OF WEEK
  23:59:59 12 - 31 - 99 - 7
- 4-BIT DATA BUS
- 4-BIT ADDRESS
- Read, Write, Hold, Chip select inputs
- Interrupt signal outputs—1024, 1, 1/60, 1/3600 Hz
- 32.768 KHz crystal controlled operation
- Leap year register bit
- 12 or 24 hour format
- ± 30 second error correction
- Single 5 volt power supply
- Back-up battery operation to V_{CC} = 2.2 V
- Low Power Dissipation
  90 μw Max. at V_{CC} = 3 V
  2.5 mw Max. at V_{CC} = 5 V
- High Density 300 mil 18-Pin Package

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



A0 to A3: Address Inputs

WRITE: Write Enable

READ: Read Enable

HOLD: Count Hold Enable

CS: Chip Select

D0 to D3: Data Input/Output

TEST: Test Input

± 30 ADJ: ± 30 Second Correction Input

XT & $\overline{XT}$: xtal oscillator connections

V_{CC}: + 5 V Supply

GND: Ground

FUNCTION TABLE

FIGURE 1

ADDRESS INPUTS				INTERNAL COUNTER	DATA I/O				DATA LIMITS	NOTES
A_0	A_1	A_2	A_3		D_0	D_1	D_2	D_3		
0	0	0	0	S 1	*	*	*	*	0 ~ 9	S_1 or S_{10} are reset to zero irrespective of input data D_0~D_3 when write instruction is executed with address selection
1	0	0	0	S 10	*	*	*		0 ~ 5	
0	1	0	0	MI 1	*	*	*	*	0 ~ 9	
1	1	0	0	MI 10	*	*	*		0 ~ 5	
0	0	1	0	H 1	*	*	*	*	0 ~ 9	
1	0	1	0	H 10	*	*	†	†	0~1 / 0~2	D_2="1" for PM, D_2="0" for AM; D_3="1" for 24 hour format, D_3="0" for 12 hour format
0	1	1	0	W	*	*	*		0 ~ 6	
1	1	1	0	D 1	*	*	*	*	0 ~ 9	
0	0	0	1	D 10	*	*	†		0 ~ 3	D_2 = "1" for 29 days in month 2; D_2 = "0" for 28 days in month 2 (2)
1	0	0	1	MO 1	*	*	*	*	0 ~ 9	
0	1	0	1	MO 10	*				0 ~ 1	
1	1	0	1	Y 1	*	*	*	*	0 ~ 9	
0	0	1	1	Y 10	*	*	*	*	0 ~ 9	

(1) * data valid as "0" or "1"
blank does not exist (unrecognized during a write and held at "0" during a read)
† data bits used for AM/PM, 12/24 HOUR and leap year
(2) If D_2 previously set to "1", upon completion of month 2 day 29, D_2 will be internally reset to "0"

TYPICAL CHARACTERISTICS—Oscillator Frequency Deviations

Frequency Deviation *vs* Temperature

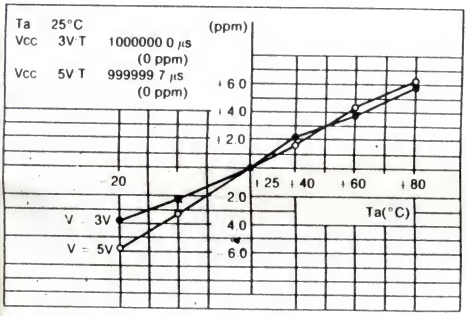


FIGURE 2

Frequency Deviation *vs* Supply Voltage

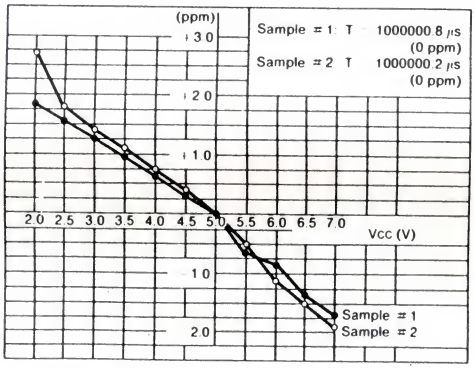


FIGURE 3

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	$-0.3 \sim 7.0$	V
Input Voltage	V_{IN}	$-0.3 \sim V_{CC} + 0.3$	V
Data I/O Voltage	V_D	$-0.3 \sim V_{CC} + 0.3$	V
Storage Temperature	T_{stg}	$-55 \sim 150$	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.75	5	5.25	V	5V ± 5%
Standby Supply Voltage	V_{CCS}	2.2	5	7	V	
Input Signal Level	V_{IH}	3.6	5	V_{CC}	V	V_{CC} = 5V ± 5% Respect to Gnd
	V_{IL}	−0.3	0	0.8	V	
Crystal Oscillator Freq.	f(XT)		32.768		KHz	
Operating Temperature	Ta	−30		+85	°C	

DC CHARACTERISTICS

(V_{CC} = 5V ± 5%; T_A = −30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Current (1)	I_{TH}	10	25	50	μA	V_{IN} = 5V
	I_{IL}	−1		1	μA	V_{IN} = 0V
Data I/O Leakage Current	I_{LD}	−1		1	μA	$V_{I/O}$ = 0 to V_{CC}, CS = "0"
Output Low Voltage	V_{OL}			0.4	V	Io = 1.6 ma, CS = "1", READ = "1"
Output Low Current	I_{OL}	1.6			mA	Vo = 0.4V, CS = "1", READ = "1"
Operating Supply Current	I_{CCS}			30	μA	V_{CC} = 3V, Ta = 25°C
	I_{CC}			500	μA	V_{CC} = 5V, Ta = 25°C

(1) XT, $\overline{XT}$ and Do∼D3 excluded.

AC CHARACTERISTICS

CAPACITANCE

T_A = 25°C, f = 1 MHz

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			5	pF

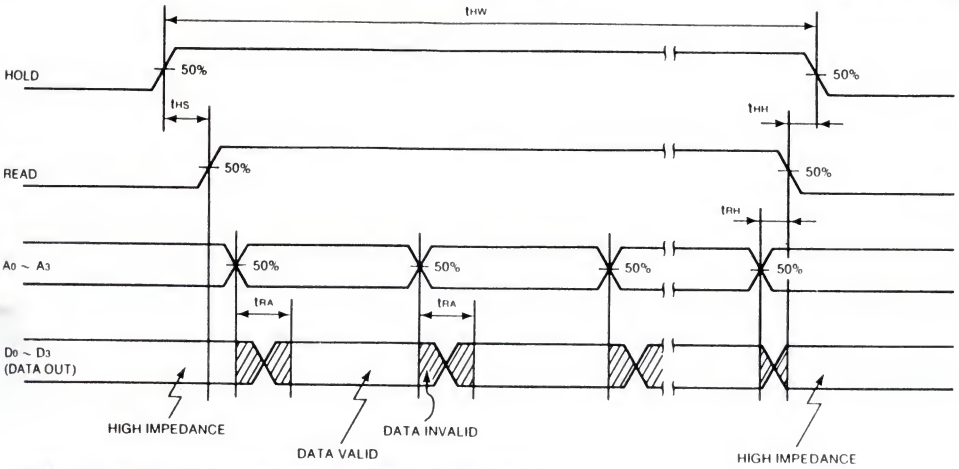
Note: This parameter is periodically sampled and not 100% tested.

READ CYCLE

(V_{CC} = 5V ± 5%; Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
HOLD Set-up Time	t_{HS}	150			μS
HOLD Hold Time	t_{HH}	0			μS
HOLD Pulse Width	t_{HW}			1	SEC
READ Hold Time	t_{RH}	0			μS
READ Access Time	t_{RA}			6	μS

READ CYCLE **FIGURE 4**



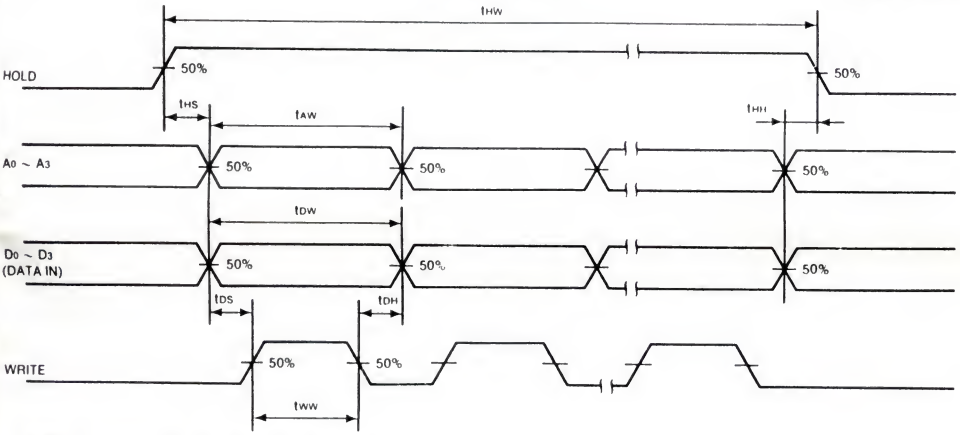
Notes: 1. A Read occurs during the overlap of a high CS and a high READ
2. Output Load: 1 TTL Gate, C_L = 50 pf and R_L = 4.7 KΩ
3. CS may be a permanent "1", or may be coincident with HOLD pulse

WRITE CYCLE

(V_{CC} = 5V ± 5%; Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
HOLD Set-up Time	t_{HS}	150			μS
HOLD Hold Time	t_{HH}	0			μS
HOLD Pulse Width	t_{HW}			1	SEC
ADDRESS Pulse Width	t_{AW}	1.7			μS
DATA Pulse Width	t_{DW}	1.7			μS
DATA Set-up Time	t_{DS}	0.5			μS
DATA Hold Time	t_{DH}	0.2			μS
WRITE Pulse Width	t_{WW}	1.0			μS

WRITE CYCLE **FIGURE 5**



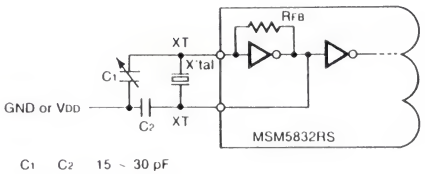
Notes: 1. A WRITE occurs during the overlap of a high CS, a high HOLD and a high WRITE
2. CS may be a permanent "1", or may be coincident with HOLD pulse

FUNCTIONAL DESCRIPTION

A block diagram of the MSM5832 microprocessor real-time clock/calendar and a package connection diagram are shown on the first page. Figure 9 illustrates a method of interfacing between the clock/calendar circuit and a micro processor. Figures 9, 10 and 11 illustrate alternative standby power supply circuits. A function table listing relationships between address inputs, data input/output and internal counter selection is shown in Figure 1. Unless otherwise indicated, the following descriptions are based on the block diagram.

32.768 K Hz OSCILLATOR (pins 16 and 17): An internal inverting amplifier with feedback resistor, R_{FB}, is connected with a crystal and two capacitors *as shown in Figure 6* to form a stable, accurate oscillator—which serves as the precision time base of the circuit. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal. Typical oscillator performance as a function of ambient temperature and supply voltage is shown in Figures 2 and 3 respectively.

OSCILLATOR CIRCUIT — FIGURE 6



C1 C2 15 ~ 30 pF

CHIP SELECT (pin 8): Connecting CS input to V_{CC} enables all inputs and outputs. Unconnected—pull-down to GND is provided by an internal resistor—or connecting CS to GND will disable HOLD, WRITE, READ, + 30 ADJ, $D_0 \sim D_3$, $A_0 \sim D_3$ and TEST.
As shown in Figure 9 CS can be used to detect system power failure by connecting system power (+ 5V) to CS, so that when system power is *on*, all inputs and outputs will be enabled, and when system power is *off*, all inputs and outputs will be disabled. The threshold voltage of CS is higher than all other inputs to insure correct operation of this function.

HOLD (pin 18): Switching this input to V_{CC} inhibits the internal 1Hz clock to the S1 counter. After the specified HOLD set-up time (150 μs), all counters will be in a static state, thus allowing error-free read or write operations. So long as the HOLD pulse width is less than 1 second, accuracy of the real time will be undisturbed. Pull-down to GND is provided by an internal resistor.

READ (pin 3): Read function *as shown in Figure 4* is enabled when READ is switched to V_{CC}. Pull-down to GND is provided by an internal resistor.

WRITE (pin 2): Write function *as shown in Figure 5* is enabled when WRITE is switched to V_{CC}. Pull-down to GND is provided by an internal resistor.

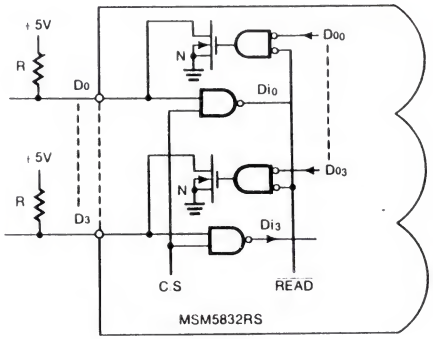
+ 30 ADJ (Pin 15): Momentarily connecting this input to V_{CC} (~31.25 ms) will reset seconds (S1, S10 counters and $2^{11} \sim 2^{15}$ frequency dividers) to 00; if seconds were 30 or more, one minute is added to the minutes (MI 1 counter) and if seconds were less than 30, the minutes are unchanged. Pull-down to GND is provided by an internal resistor.

$A_0 \sim A_3$ (pins 4 ~ 7): Address inputs, used to select internal counters for read/write operations (see function table—*Figure 1*). A "1" is defined as V_{CC}; a "0" is GND. Pull-down to GND is provided by internal resistors.

$D_0 \sim D_3$ (pins 9 ~ 12): Data Inputs/Outputs, two-way bus lines controlled by READ and WRITE inputs. *As shown in Figure 7* external pull-up resistors of 4.7K or higher are required by the open-drain N-channel MOS outputs. D_3 is the MSB; D_0 is the LSB.

TEST (pin 14): Normally this input is unconnected—pull-down to GND is provided by an internal resistor—or connected to GND. With CS at V_{CC}, pulses to V_{CC} on the TEST input will directly clock the S1, MI10, W, D1 and Y1 counters, depending on which counter is addressed (W and D1 are selected by D1 address in this mode only). Roll-over to next counter is enabled in this mode.

DATA I/O CIRCUIT — FIGURE 7



REFERENCE SIGNAL OUTPUT
Reference signals are available as outputs on $D_0 \sim D_3$ if CS, READ and $A_0 \sim A_3$ are at V_{CC}. Refer to *Figure 8* for specifics. *As shown in Figure 9* these signals may be used to generate interrupts for the microprocessor.

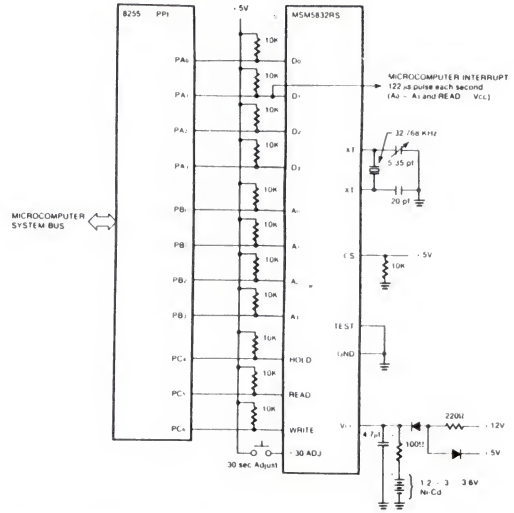
REFERENCE SIGNAL OUTPUTS — FIGURE 8

CONDITIONS	OUTPUT	REFERENCE FREQUENCY	PULSE WIDTH
HOLD = L	D_0 (1)	1024 Hz	duty 50%
READ = H	D_1	1 Hz	122.1 μs
C.S. = H	D_2	1/60 Hz	122.1 μs
$A_0 \sim A_3$ = H	D_3	1/3600 Hz	122.1 μs

(1) 1024 Hz signal at D_0 not dependent on HOLD input level

TYPICAL APPLICATION—Use with Programmable Peripheral Interface (PPI)

FIGURE 9



TYPICAL APPLICATIONS—Alternative Standby Power Supply Circuits

FIGURE 10

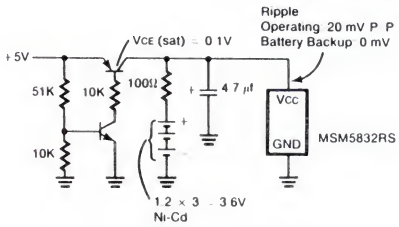
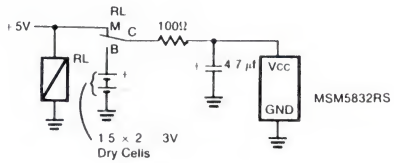
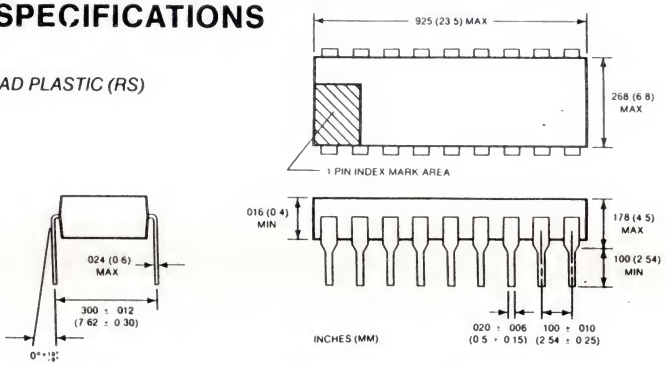


FIGURE 11



PACKAGE SPECIFICATIONS

18 LEAD PLASTIC (RS)



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JK AUDIO

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1-619-555-1212

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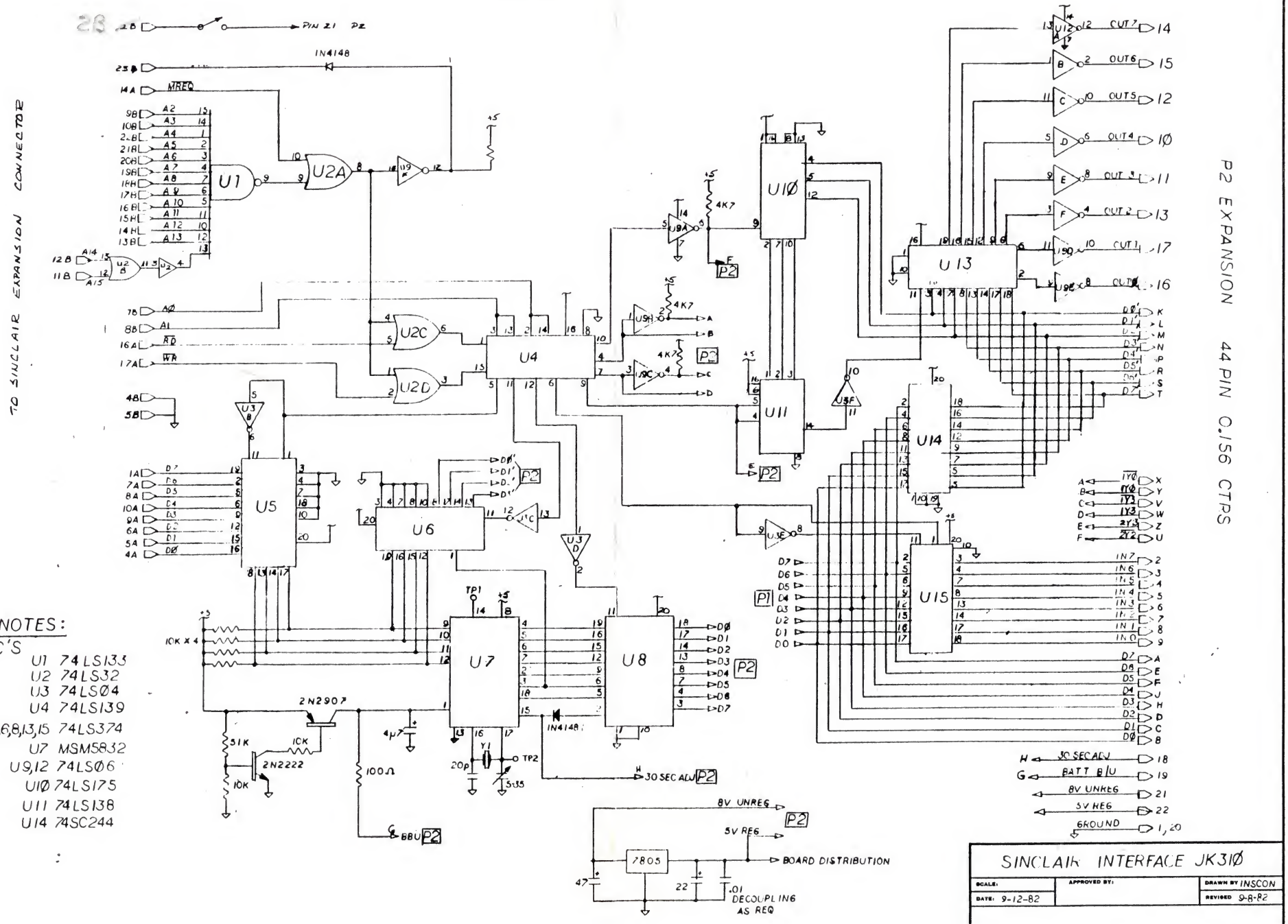
TO SINCLAIR EXPANSION CONNECTOR
P2 EXPANSION 44 PIN C/156 CTRS
IN4148
MREQ
U1
U2A
U2C
U2D
U4
U5
U6
U7
U8
U10
U11
U12
U13
U14
U15
4K7
2N2907
2N2222
51K
10K
100Ω
4µ7
20p
Y1
TP1
TP2
7805
47
22
.01
DECOUPLING AS REQ
8V UNREG
5V REG
BOARD DISTRIBUTION
BBU
30 SEC ADV
BATT B/U
GROUND
NOTES:
①IC'S
U1 74LS133
U2 74LS32
U3 74LS04
U4 74LS139
U5,6,8,13,15 74LS374
U7 MSM5832
U9,12 74LS06
U10 74LS175
U11 74LS138
U14 74SC244
SINCLAIR INTERFACE JK310
SCALE:
APPROVED BY:
DRAWN BY INSCON
DATE: 9-12-82
REVISED 9-8-82
DRAWING NUMBER
31001